USP - ICMC - SSC
SCE 0703 (PISE) - 2o. Semestre 2008

Disciplina de Projeto e Implementação de Sistemas Embarcados I

Prof. Fernando Santos Osório
Email: fosorio [at] { icmc. usp. br , gmail. com }
Web: http://www.icmc.usp.br/~fosorio/

Aula 02

Aula 02 - FPGA e Ferramentas

Agenda:

1. **Projeto de Sistemas Embarcados**
2. **Projeto de Hardware Reconfigurável**
   Programmable Logic Devices
3. **FPGA - Field Programmable Gate Array**
   - **3.1 Altera - Kits de Desenvolvimento: Cyclone**
4. **Altera FPGA**
   - **4.1 Ferramentas de Desenvolvimento: Quartus II, ModelSim / Nios II**
   - **4.2 Quartus II**
5. **Aplicações**

1. Projeto de Sistemas Embarcados

Sistemas Embarcados

- Especificação do produto e seus Requisitos
- Especificação e Implementação do Hardware
- Grande variedade de Plataformas de Hardware

> Microprocessador (CISC, RISC, Multi-Core, SIMD, VLIW)
> Microcontrolador
> Processador DSP
> Dispositivos FPGAs e CLPDs
> SoC /SoPC - *System on a (Programmable) Chip*
ASIP - *Application Specific Instruction Set Processors*
> ASIC - *Application Specific Integrated Circuit*
> Circuito dedicado

Questões: Custo, Consumo, Dimensões, Periféricos,
Desempenho, Confiabilidade...

Importância: **Avaliação do HW!**
Ferramentas de apoio ao desenvolvimento!

USP - SCE-703 - 2008-2
Proj. e Implem. de Sistemas Embarcados I
Prof. Fernando Osório

1. Projeto de Sistemas Embarcados

Sistemas Embarcados

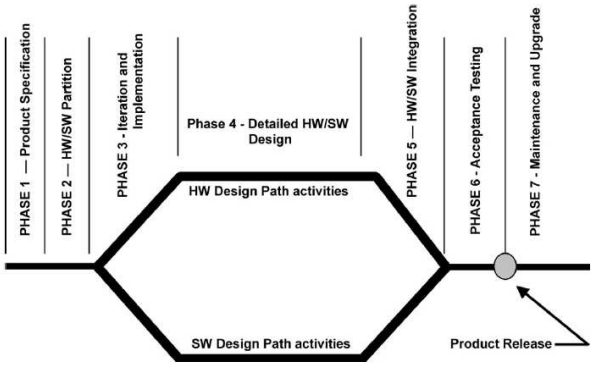


Figure 1.1: Embedded design life cycle diagram.

Exemplos de aplicações:
- Robôs HOAP(Fujitsu), Khepera(K-Team), E-Puck(K-Team), Pioneer(ActivMedia), QuadRover(Parallax), ...
- MP3 Players, iPods, PDAs, Cell Phones, Digital Cameras, ...

1. Projeto de Sistemas Embarcados

Sistemas Embarcados - Exemplo do ARMUS

ARMUS, an ARM Robotic Processing System for Educational Purposes
Site: http://www.opencircuits.com/ARMUS_Embedded_Linux_Board

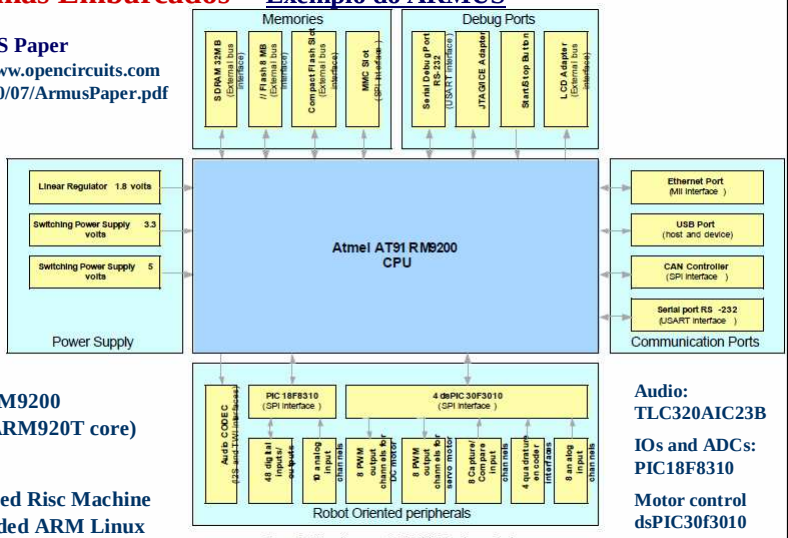
Specs - The board is made to run Linux (ran Linux 2.4 with no big issues).

* AT91RM9200 CPU (ARM920T core)
* On board 32MB SDRAM and 8 MB Flash.
* CompactFLash
* SD/MMC trough SPI
* 2 RS232 ports
* JTAG/ICE port
* LCD port on the memory bus, we used a graphical LCD of 64x128
* 10baseT Ethernet
* USB Host and Device
* CAN port
* Audio (TLC320AIC23B: stereo out, stereo in, microphone in, 44.1kHz 16 bits)
* 48 IOs and 10 ADCs on a PIC18F8310
* 4x dsPIC30f3010 for motor control
  (4 DC, 4 servo, 4 capture/compare, 4 quad encoder, 8 more ADCs)
* Power with two switching power supplies (3.3V and 5V) to minimize power comsuption.

1. Projeto de Sistemas Embarcados

Sistemas Embarcados - Exemplo do ARMUS

ARMUS Paper
http://www.opencircuits.com
/images/0/07/ArmusPaper.pdf



AT91RM9200
CPU (ARM920T core)

ARM
Advanced Risc Machine
Embedded ARM Linux

Audio:
TLC320AIC23B

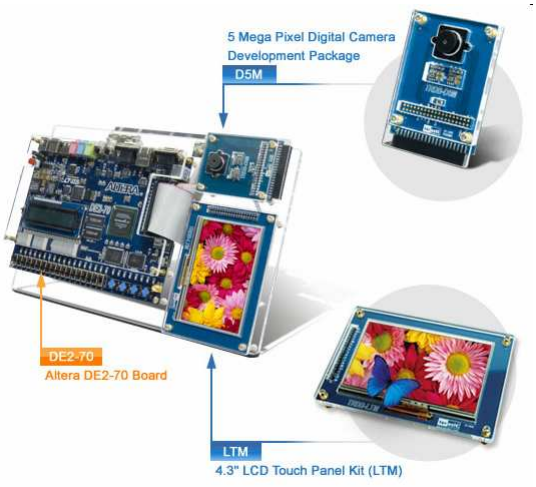
IOs and ADCs:
PIC18F8310

Motor control
dsPIC30f3010

Figure 1: Bloc diagram of ARMUS' hardware design.

1. Projeto de Sistemas Embarcados

Sistemas Embarcados - **Exemplo do DE2-70 / DM5 / LTM**



Site: http://www.terasic.com.tw/cgi-bin/page/archive.pl?CategoryNo=39

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices (PLDs / CPLDs)

Tipo de Dispositivos Lógicos Programáveis - [Simple/Complex]PLDs

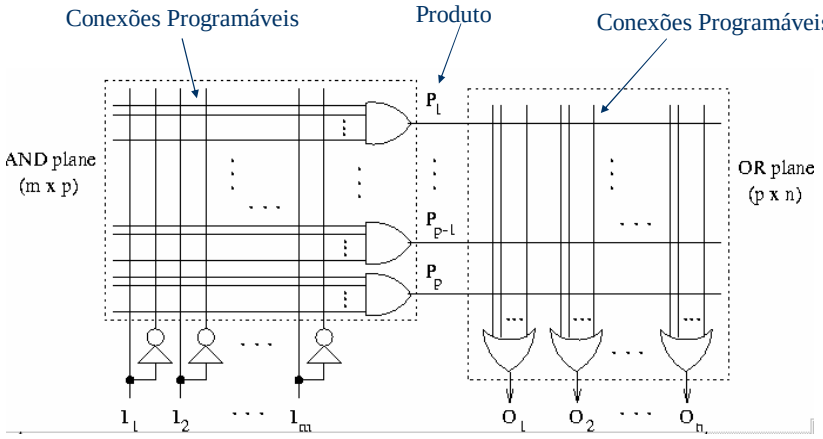
- **Programmable Logic Array (PLA)**
- **Programmable AND-Array Logic (PAL)**
- **Generic Array Logic (GAL)**
- **PAL, Configurable and Erasable (PALCE)**
- **Field Programmable Gate Array (FPGA)**
- **Programmable Read-Only Memory (PROM)**

Fonte/Refs.: S. Lee - http://www.postech.ac.kr/class/cs311/ (downloads)
S. Brown and J. Rose - http://www.eecg.toronto.edu/~brown/papers/DandT-FPGA-CPLD.html
http://portal.acm.org/citation.cfm?id=622676

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices (PLDs / CPLDs)

Programmable Logic Array (PLA) - Estrutura Lógica



Expressão: Soma dos Produtos

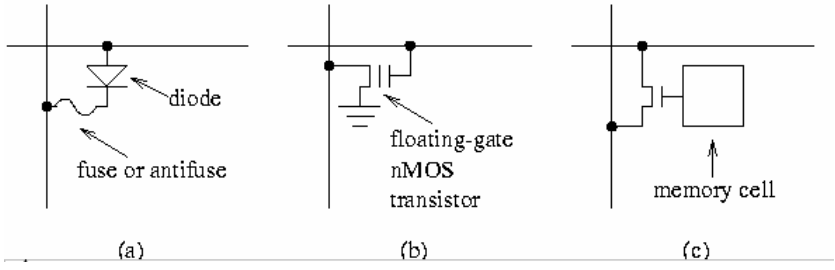
Fontes.: S. Lee / S.Brown and J. Rose

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices (PLDs / CPLDs)

Programmable Logic Array (PLA) - Métodos de Programação das Conexões

Usando um programador de PLD (ROM writer)
para programar um PLA: determinar onde as conexões serão feitas.



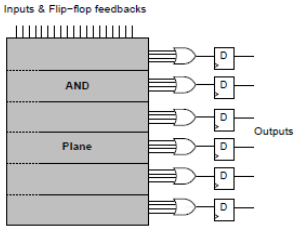
Fontes.: S. Lee / S.Brown and J. Rose

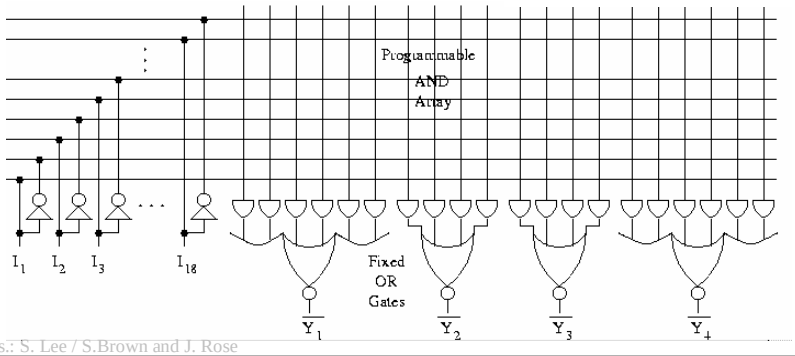
2. Projeto de Hardware Reconfigurável

Programmable Logic Devices

Programmable AND-Array Logic - PAL

PAL- Programmable Array Logic (PAL) is a relatively small FPD that has a programmable AND-plane followed by a fixed OR-plane [PAL is a trademark of Advanced Micro Devices]





Fontes.: S. Lee / S.Brown and J. Rose

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices

Field Programmable Gate Arrays - FPGA

- A maioria dos tipos de chips complexos pode ser "programado" para implementar circuitos arbitrários;
- Diferentes fabricantes competindo entre si: Actel, Altera, Cypress, Lattice, Xilinx, etc.
- Fatores competitivos:
  - Grande nro. de portas lógicas;
  - Velocidade dos dispositivos;
  - Flexibilidade e Custo;
  - Reprogramabilidade;

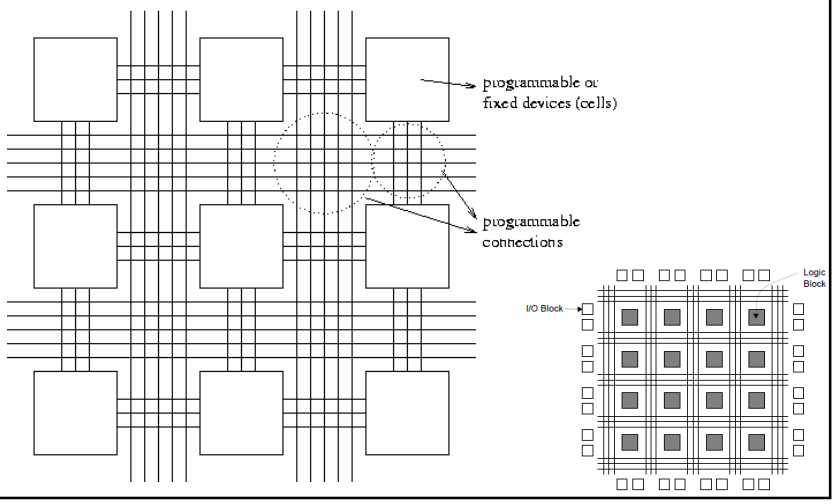
> FPGA: um array programável de PLDs simples
> FPGA: field programmable version of “gate array”

Fontes.: S. Lee / S.Brown and J. Rose

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices

FPGA: Estrutura Básica de um Gate Array



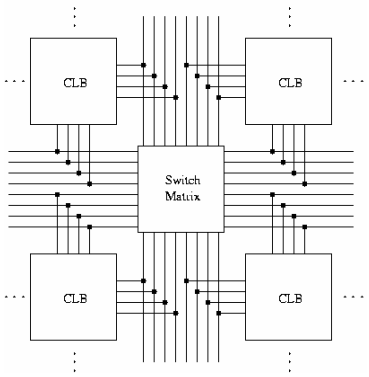
3. FPGA - Field Programmable Gate Array

FPGA - Conceitos Básicos e Nomenclatura

ASIC - Application Specific Integrated Circuit
ASIP - Application Specific Instruction Set Processors
CPLD - Complex Programmable Logic Devices
FPGA - Field Programmable Gate Array
FPGA CLB - FPGA Combinatorial Logic Block
FPGA LE - FPGA Logical Element
FPD - Field Programmable Device
HDL - Hardware Description Language
JTAG - Joint Test Action Group (Standard test access port and boundary-scan architecture)
IP / Cores - Intellectual Property **IEEE 1149.1 Standard**
PLA/PAL - Programmable Logic Array
PLD - Programmable Logic Device
SOC/SOPC - System-on-a-Chip / System-on-a-Programmable-Chip
VERILOG - Verilog HDL
VHDL - VHSIC (Very High Speed Integrated Circuits) Hardware Description Language

FPGA - XC4010XL Xilinx FPGA Block Diagram

FPGA: CLB + Interconnection Logic
CLB = Combinatorial/Configurable Logic Block (Elemento básico)



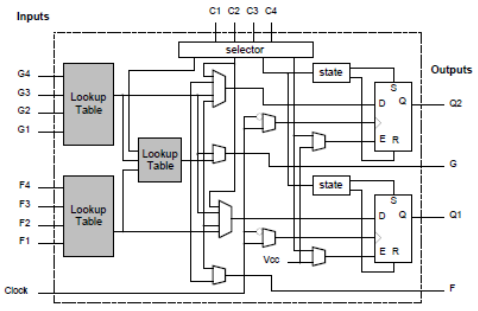
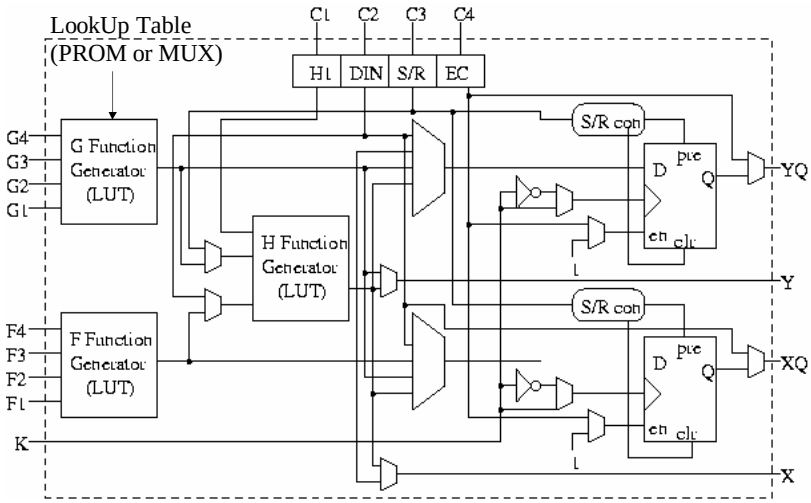


Figure 18 - *Xilinx XC4000 Configurable Logic Block (CLB).*

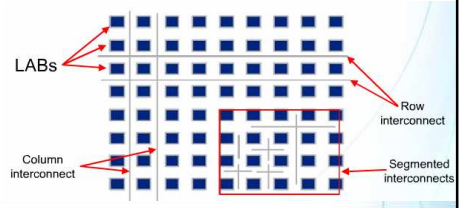
FPGA - XC4010XL Xilinx FPGA - CLB Block Diagram

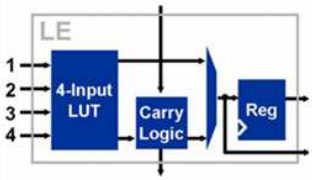


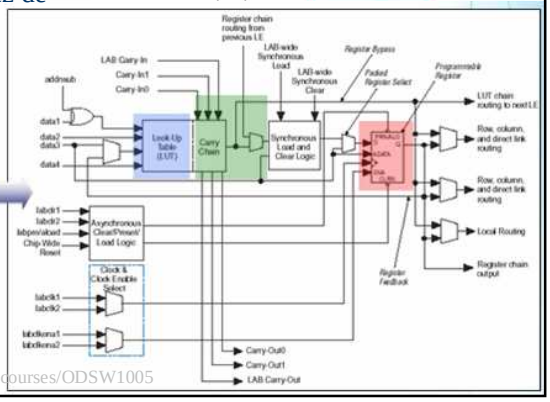
3. FPGA - Field Programmable Gate Array

FPGA - **Altera FPGA**

Altera CLPDs => FPGA
LAB - Logic Array Blocks
FPGA LAB composto de
Logic Elements (LE), em vez de
Produto de Termos
e MacroCélulas







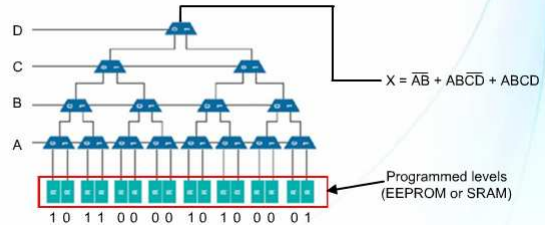
Material Complementar:
Altera FPGA Curso On-Line
http://www.altera.com/education/training/courses/ODSW1005

3. FPGA - Field Programmable Gate Array

FPGA - **Altera FPGA**

Altera CLPDs => FPGA
LAB - Logic Array Blocks
FPGA LAB composto de Logic Elements (LE)
Logic Element LUTs,

LUT inputs are mux select lines



3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA - Cyclone EP1C**

Table 1. Cyclone Device Overview

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Logic Elements (LEs)	2,910	4,000	5,980	12,060	20,060
M4K RAM Blocks (4 Kbits + parity)	13	17	20	52	64
Total RAM Bits	59,904	78,336	92,160	239,616	294,912
Phase-Locked Loops (PLLs)	1	2	2	2	2
Maximum User I/O Pins	104	301	185	249	301
Production Device Availability	April 2003	September 2003	Now	Now	Now

Cyclone™ microtronix ALTERA firefly Configurable Processor Module

Hardware - SCE 703:
Cyclone I - EP1C12F324C8
Firefly Board
NIOS II

Site Altera Cyclone: http://www.altera.com/products/devices/cyclone/cyc-index.jsp

USP - SCE-703 - 2008-2
Proj. e Implem. de Sistemas Embarcados I
Prof. Fernando Osório

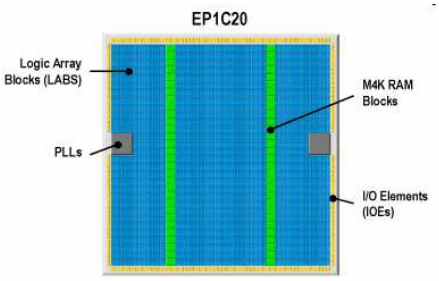
3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA - Cyclone EP1C20

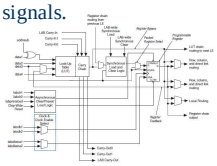
Cyclone Architecture

Abundant logic and memory resources, clock management circuitry, and advanced I/O capabilities are all available in Cyclone devices. The Cyclone architecture consists of vertically arranged Logic Elements (LEs), embedded memory blocks, and phase-locked loops (PLLs) that are surrounded by I/O elements (IOEs). A highly efficient interconnect and low-skew clock network provide connectivity between each of these structures for clock and data signals.

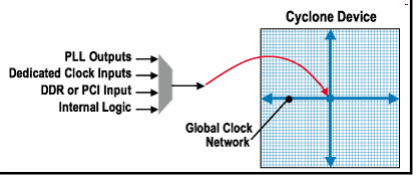
EP1C20 Device Floorplan



Cyclone LE Logic Element



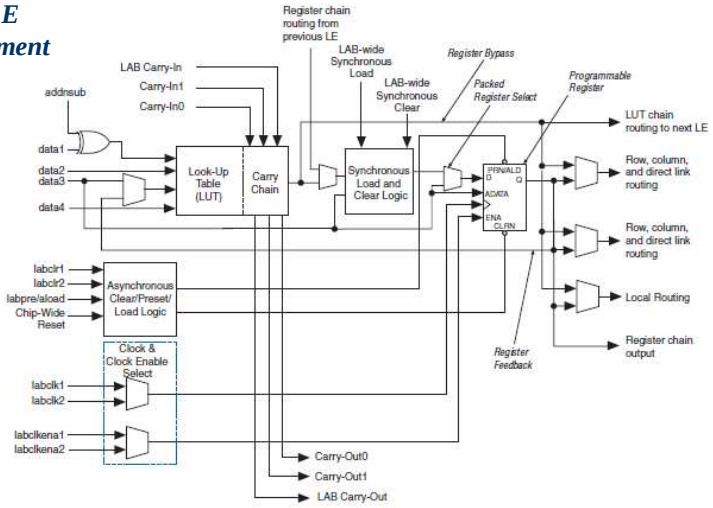
Cyclone Device Clock Network



3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA - Cyclone EP1C20

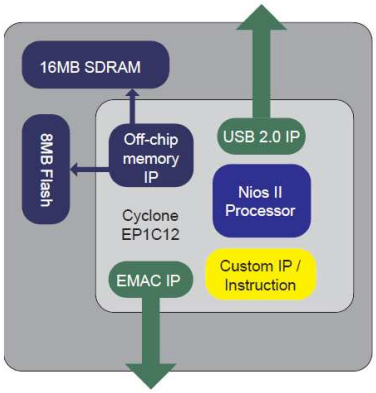
Cyclone LE
Logic Element



3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA - Cyclone EP1C12 Kit - Firefly

Firefly module



Firefly Configurable Processing Modules add FPGA flexibility and 32-bit RISC processing power to your next embedded product.

Firefly modules can be designed to fit any number of embedded device requirements.

Site Microtronix Firefly: http://www.microtronix.com/downloads/?product_id=88

4. Altera FPGA

Ferramentas de Desenvolvimento

Ferramentas de Software

Quartus II 6.0-8.0
ModelSim-Altera Edition
SOPC Builder and IP Solutions
Nios II Integrated Development Environment (IDE) - Cyclone Edition

Player/Stage (Robot Simulation - Pioneer 3 DX/AT)

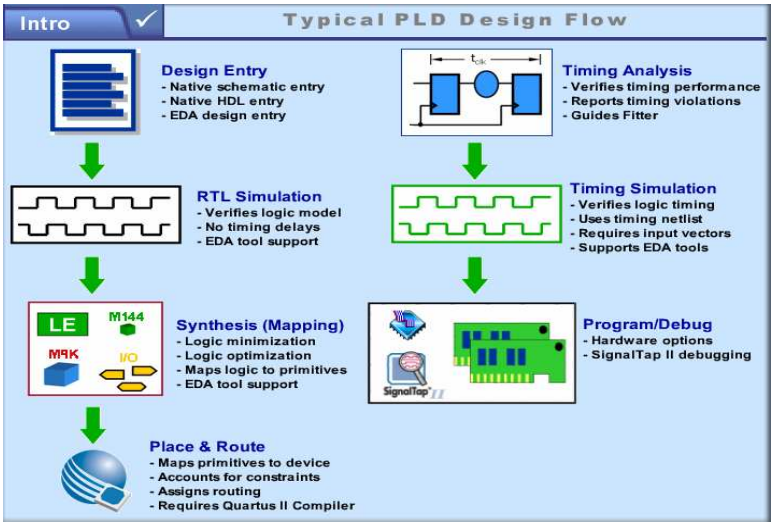
Ferramentas de Hardware

Altera FPGA EP1C12F324C98
Cyclone / Firefly Board
NIOS II Evaluation Board Kit

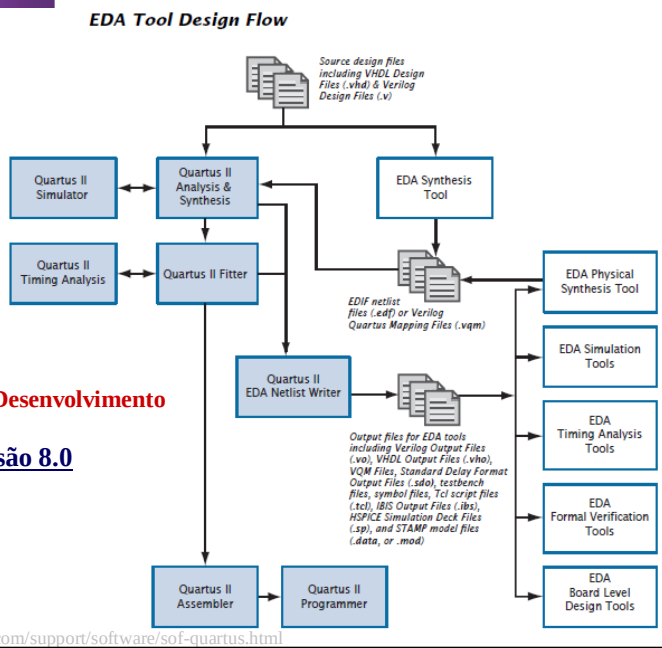
Pionner 3 DX/AT Robots

4. Altera FPGA

Ferramentas de Desenvolvimento



4. Altera FPGA



Ferramentas de Desenvolvimento

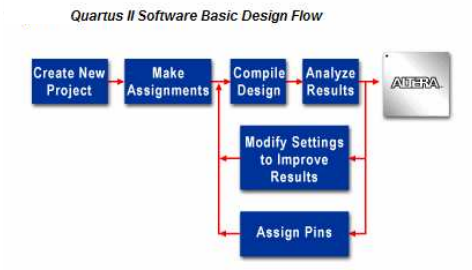
Quartus II Versão 8.0

Site http://www.altera.com/support/software/sof-quartus.html

4. Altera FPGA

Ferramentas de Desenvolvimento

Quartus II Versão 8.0

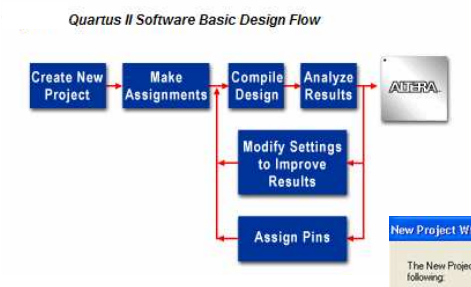


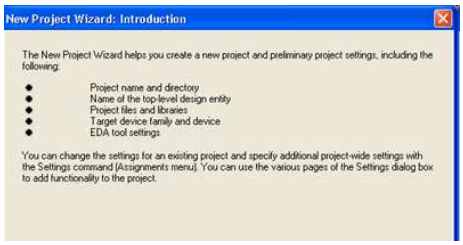
Site http://www.altera.com/support/software/sof-quartus.html

4. Altera FPGA

Ferramentas de Desenvolvimento

Quartus II Versão 8.0



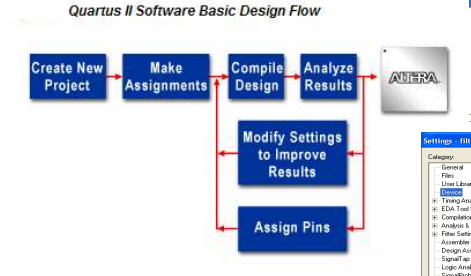


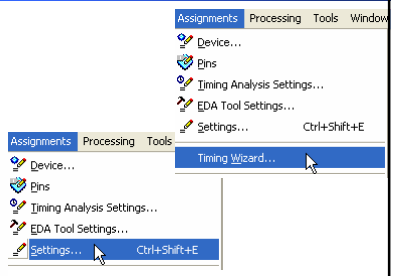
>> New Project Wizard

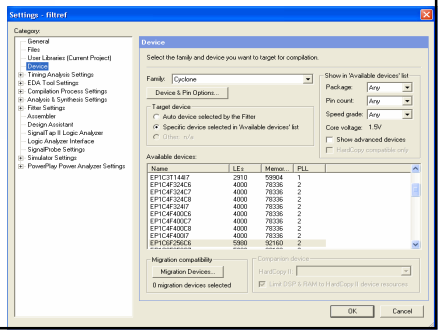
4. Altera FPGA

Ferramentas de Desenvolvimento

Quartus II Versão 8.0





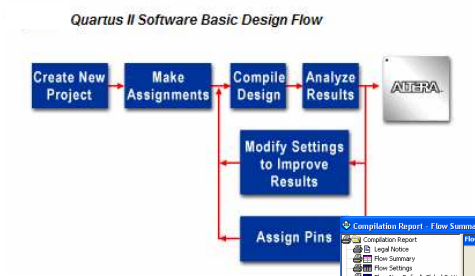


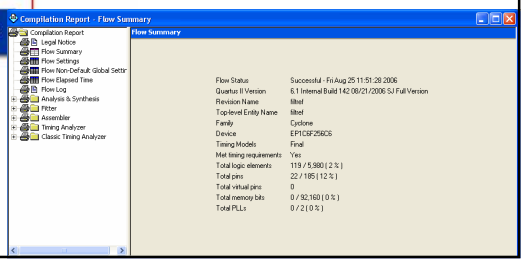
>> Assignments Menu:
Settings, Timing

4. Altera FPGA

Ferramentas de Desenvolvimento

Quartus II Versão 8.0



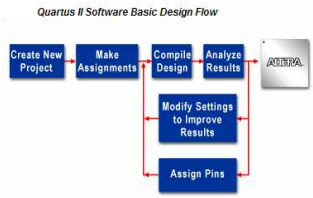


>> Compile Design and
Analyze Results

USP - SCE-703 - 2008-2
Proj. e Implem. de Sistemas Embarcados I
Prof. Fernando Osório

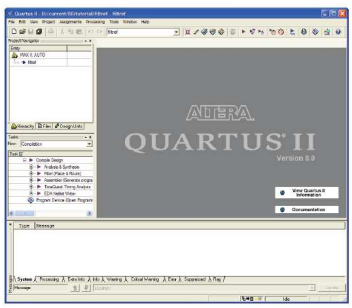
4. Altera FPGA

Quartus II Versão 8.0



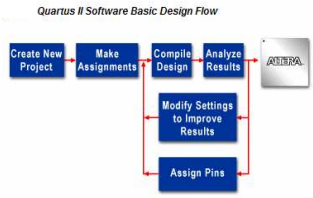
Steps:

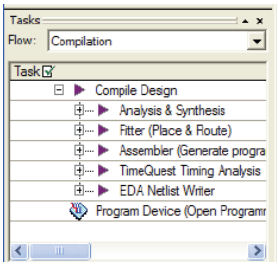
1. Create New Project
   New Project Wizard
   > Add Files (vhd, v)
   > Create Block Diagram Schematic File
   Block Editor (bdf)
   MegaFunctions (MegaWizard)
   > Add Pins
2. Make Assignments
   Settings (clock speed)
   Timing Wizard
   > Assignment Editor
   > Timing Analysis
3. Compile Design
4. Analyze Results
5. Modify Settings to Improve Results (Timing Analysis)
6. Assign Pins (Assignment Editor)



4. Altera FPGA

Quartus II Versão 8.0





Steps:

1. Create New Project
   New Project Wizard
   > Add Files (vhd, v)
   > Create Block Diagram Schematic File
   Block Editor (bdf)
   MegaFunctions (MegaWizard)
   > Add Pins
2. Make Assignments
   Settings (clock speed)
   Timing Wizard
   > Assignment Editor
   > Timing Analysis
3. **Compile Design**
4. Analyze Results
5. Modify Settings to Improve Results (Timing Analysis)
6. Assign Pins (Assignment Editor)

USP - SCE-703 - 2008-2
Proj. e Implem. de Sistemas Embarcados I
Prof. Fernando Osório

4. Altera FPGA

Quartus II Versão 8.0 - TUTORIAL

INFORMAÇÕES SOBRE A DISCIPLINA

USP - Universidade de São Paulo - São Carlos, SP
ICMC - Instituto de Ciências Matemáticas e de Computação
SSC - Departamento de Sistemas de Computação

Prof. Fernando Santos OSÓRIO
Web institucional: http://www.icmc.usp.br/ssc/
Página pessoal: http://www.icmc.usp.br/~fosorio/
E-mail: fosorio [at] icmc. usp. br ou fosorio [at] gmail. com

Disciplina de Proj. e Implementação de Sistemas Embarcados I
Ferramentas: Altera - Quartus, NIOS II, Cyclone Dev-Kit
Web disciplina: Http://www.icmc.usp.br/~fosorio/
> Programa, Material de Aulas, Critérios de Avaliação,
> Material de Apoio, Trabalhos Práticos