

**USP - ICMC - SSC
SCE 0703 (PISE) - 2o. Semestre 2008**

Quartus II Versão 8.0 - TUTORIAL

Prof. Fernando Santos Osório
Email: fosorio [at] { icmc. usp. br , gmail. com }
Web: <http://www.icmc.usp.br/~fosorio/>

Quartus II Versão 8.0 - TUTORIAL

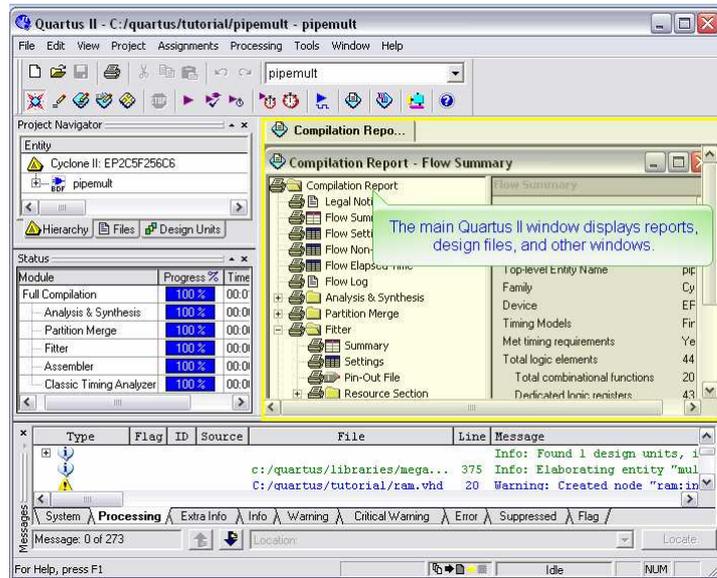


Intro ✓ **Tutorial Modules**

Select one of the following tutorial modules:

-  Module 1: Quartus II Introduction
(5 minutes)
-  Module 2: Create a Design
(30 minutes)
-  Module 3: Compile a Design
(40 minutes)
-  Module 4: Run Timing Analysis
(40 minutes)
-  Module 5: Run Timing Simulation
(30 minutes)
-  Module 6: Configure a Device
(20 minutes)
-  Module 7: Advanced Topics
(20 minutes)

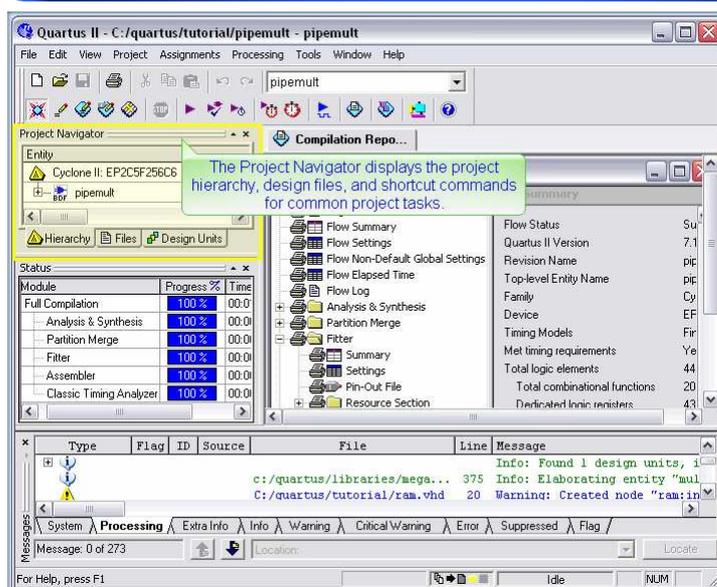
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QUARTUS II
INTERFACE

> Main Window

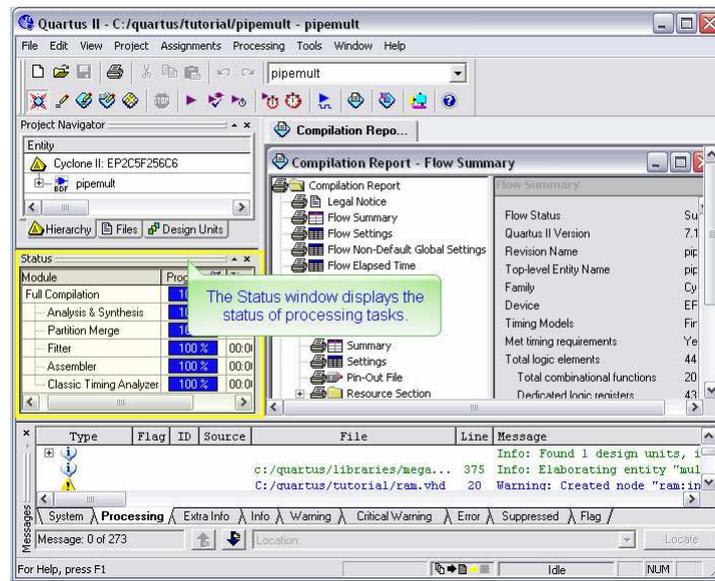
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QUARTUS II
INTERFACE

> Project
Navigator

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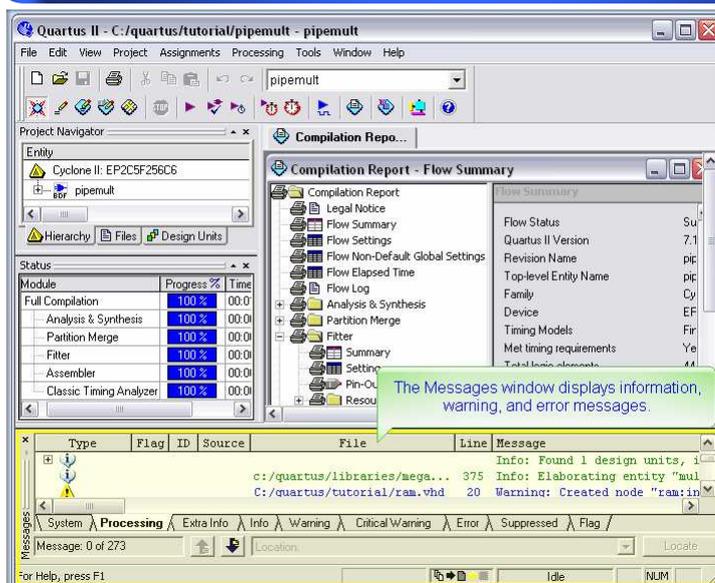


QUARTUS II
INTERFACE

> Status
Window

5
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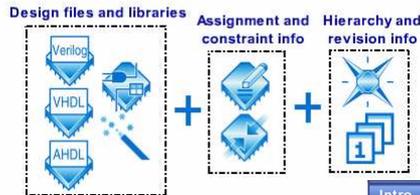


QUARTUS II
INTERFACE

> Messages
Window

6
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Quartus II Projects include:



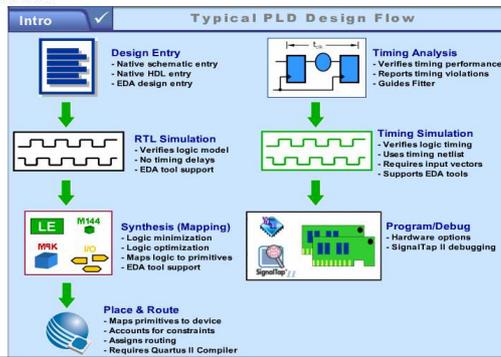
QUARTUS II

> Projects:

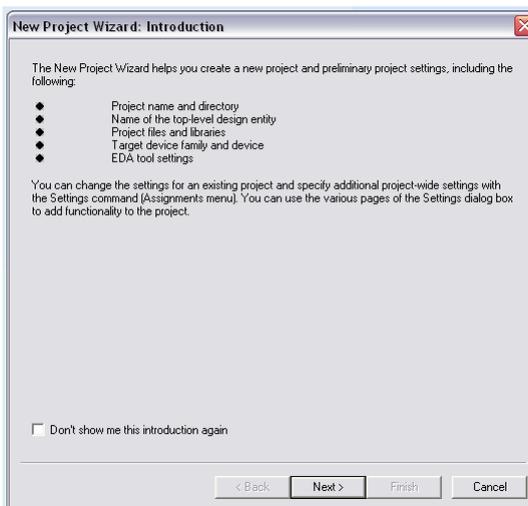
QPF - Quartus Project File
QSF - Quartus Settings File

> Wizard

Helps to Create new projects



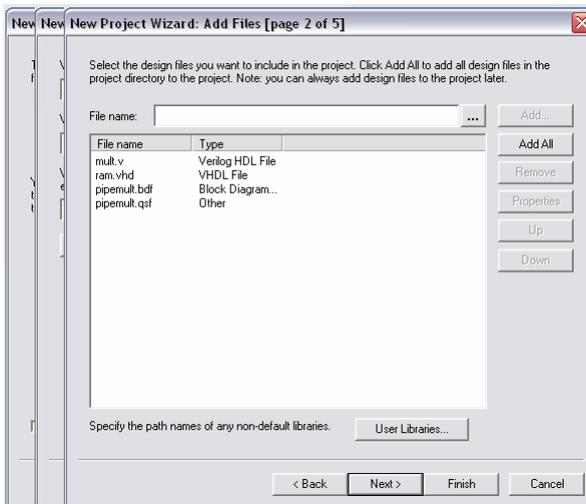
QUARTUS II - Wizard: Helps to Create new projects



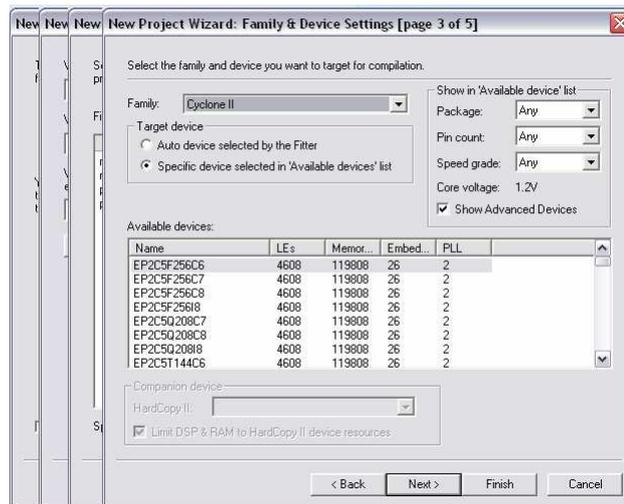
QUARTUS II - Wizard: Helps to Create new projects



QUARTUS II - Wizard: Helps to Create new projects



QUARTUS II - Wizard: Helps to Create new projects

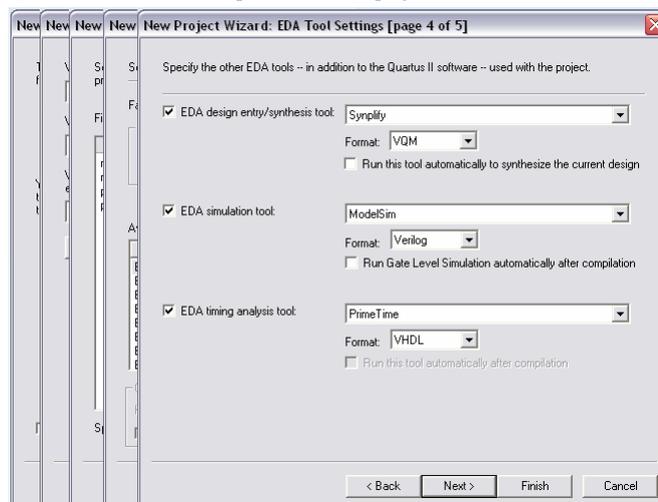


11

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Target Altera Device

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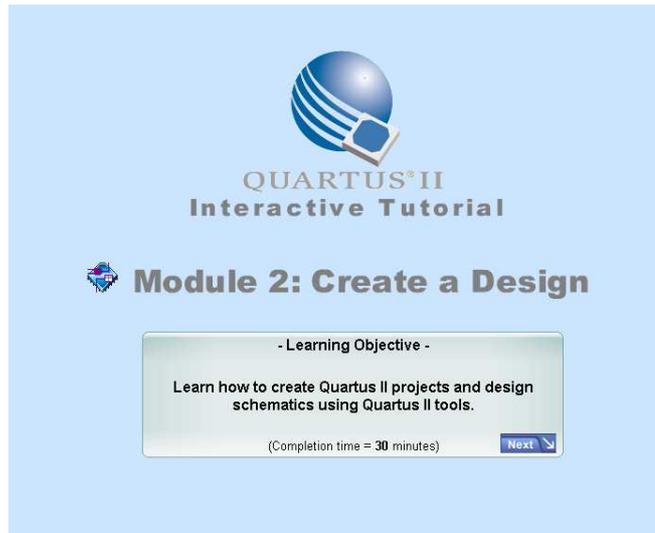


12

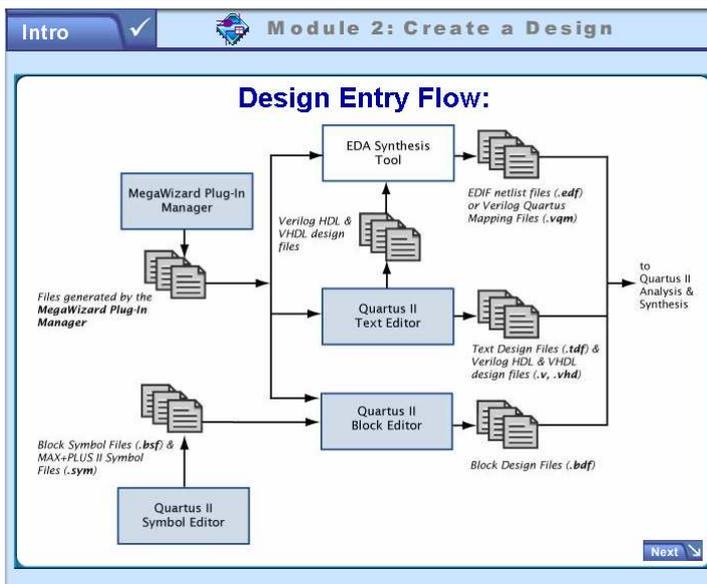
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EDA Tool Settings

QUARTUS II - Create a Design



The screen displays the Quartus II logo at the top, followed by the text "QUARTUS® II Interactive Tutorial". Below this is the title "Module 2: Create a Design" with a small icon. A central box contains the learning objective: "Learn how to create Quartus II projects and design schematics using Quartus II tools." Below the objective, it states "(Completion time = 30 minutes)" and a "Next" button with a dropdown arrow.



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Intro **Module 2: Create a Design**

This tutorial uses the following pipelined multiplier design to teach you how to create a schematic design:

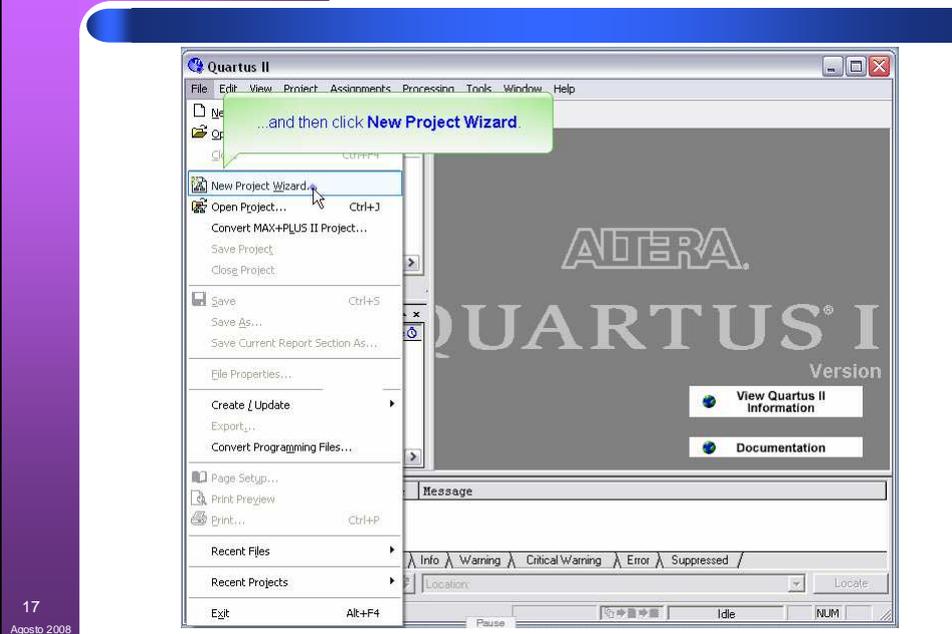
[Next](#)

15
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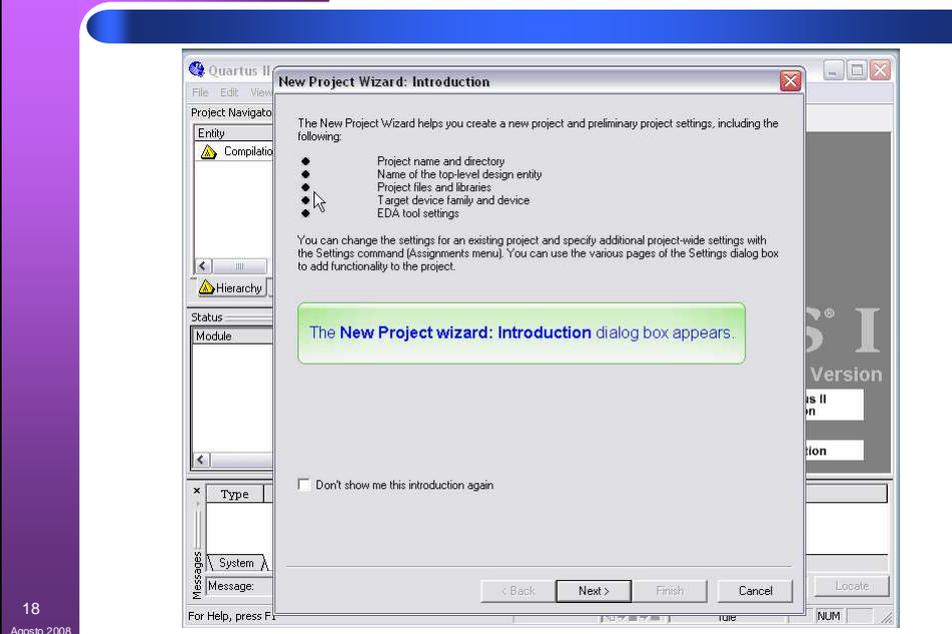
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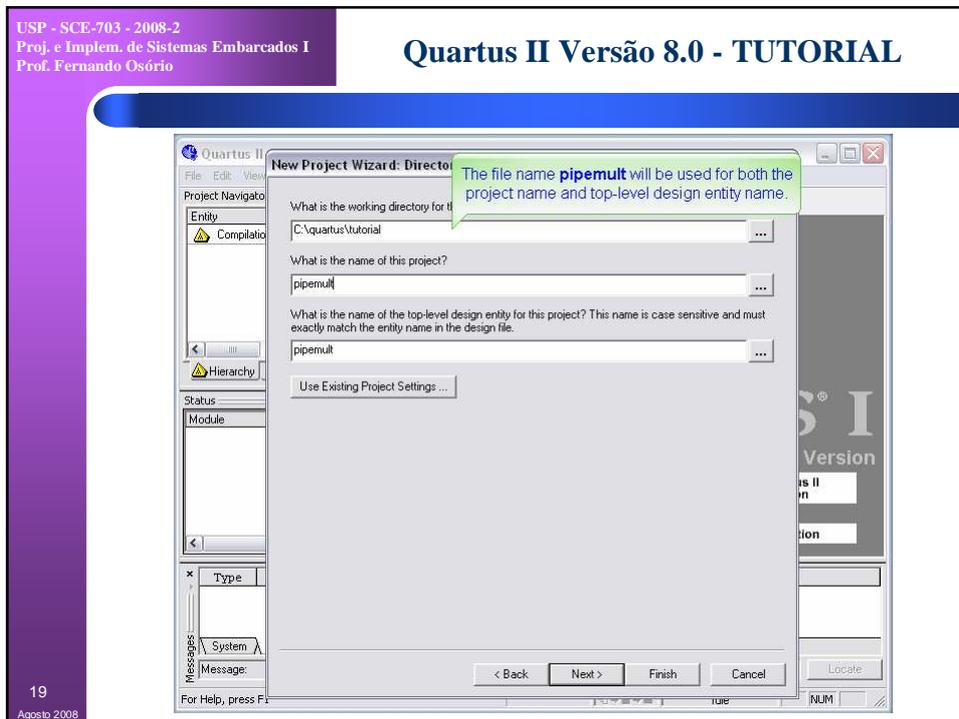
16
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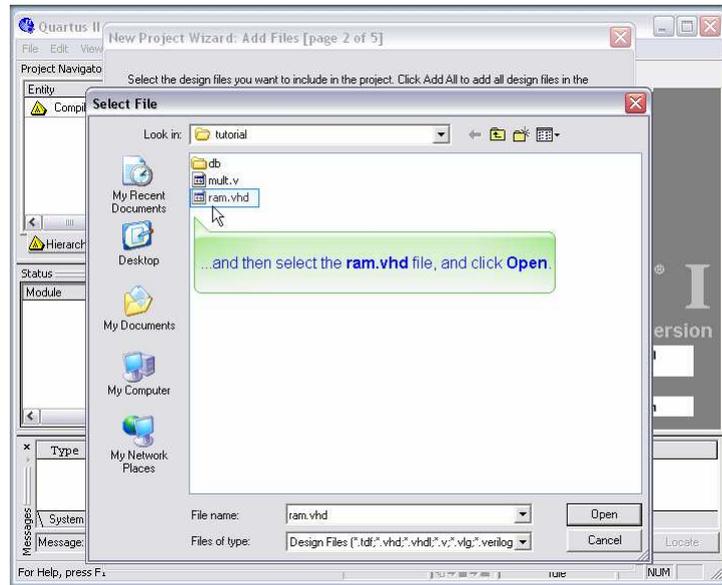
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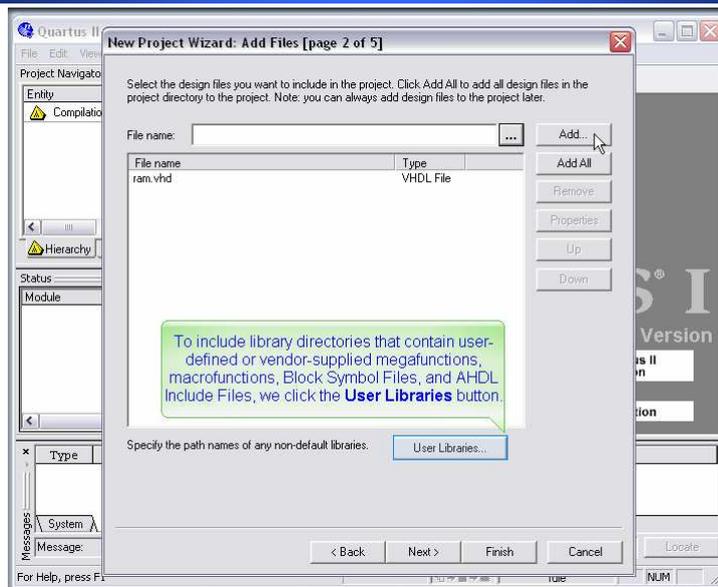
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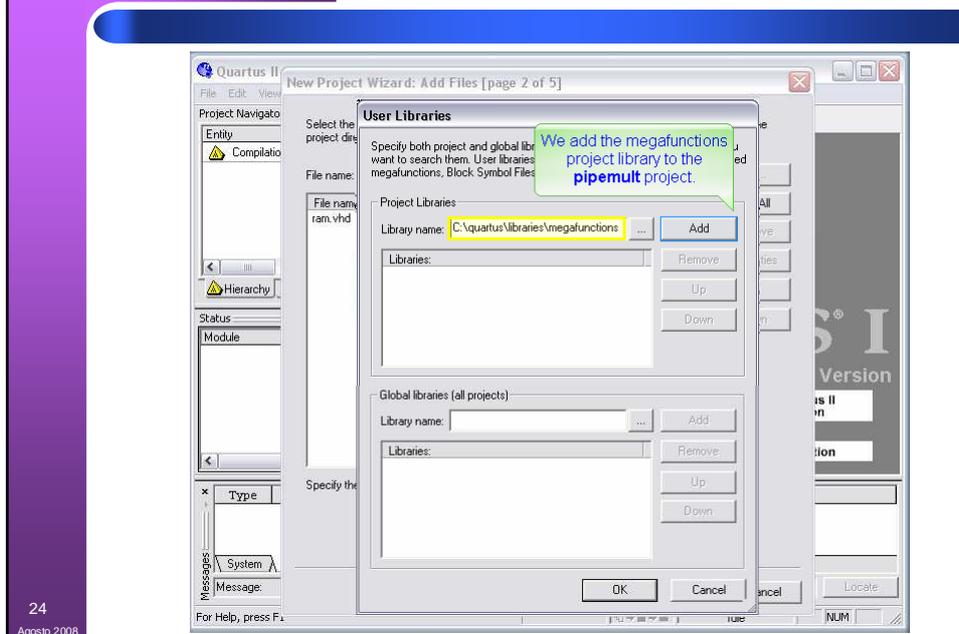
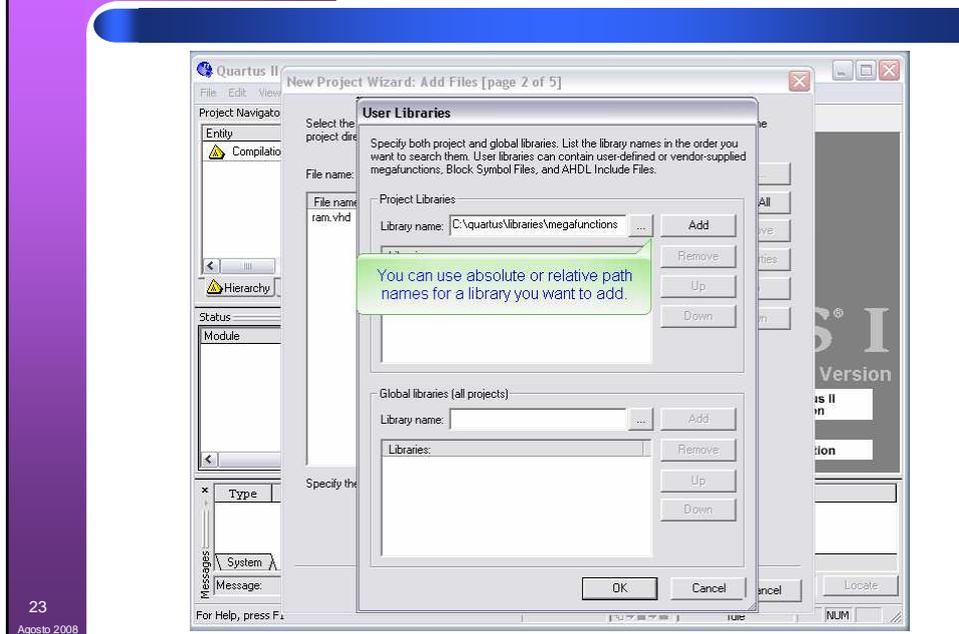
21
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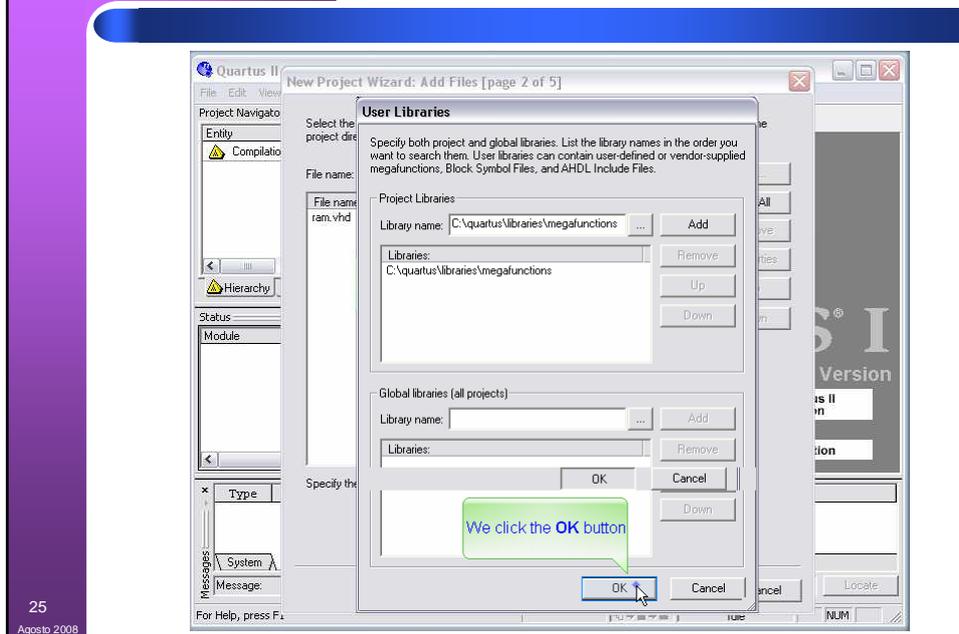


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22
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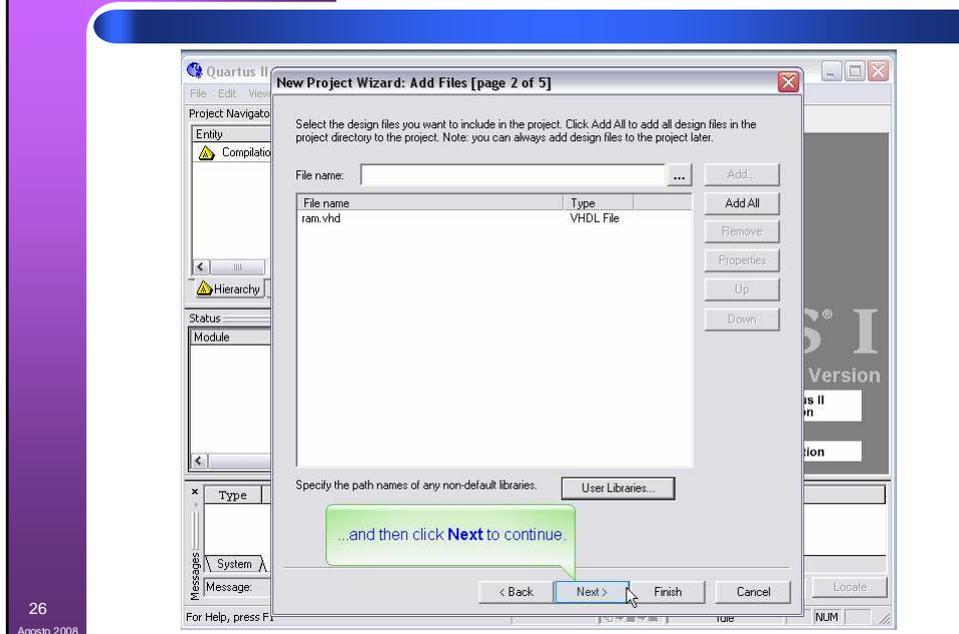






25

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26

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New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Family: Cyclone

Target device:
 Auto device selected by the Filter
 Specific device selected in 'Available devices' list

Available devices:

Name	LEs	Memor...	PLL
EP1C3T100C6	2910	59904	1
EP1C3T100C7	2910	59904	1
EP1C3T100C8	2910	59904	1
EP1C3T100C9	2910	59904	1
EP1C3T100D7	2910	59904	1
EP1C3T144C6	2910	59904	1
EP1C3T144C7	2910	59904	1
EP1C3T144C8	2910	59904	1
EP1C3T144I7	2910	59904	1
EP1C4F324C6	4000	78336	2
EP1C4F324C7	4000	78336	2

Package: Any
 Pin count: Any
 Speed grade: Any
 Core voltage: n/a
 Show advanced devices
 HardCopy compatible only

Companion device:
 HardCopy II:
 Limit DSP & RAM to HardCopy II device resources

< Back Next > Finish Cancel

The Family & Device Settings page allows us to specify the target device for compilation.

27

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New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Family: Cyclone II

Target device:
 Auto device selected by the Filter
 Specific device selected in 'Available devices' list

Available devices:

Name	LEs	User I/...	Memor...	Embed...	PLL	Global...
EP2C5F256C6	4608	170	119808	26	2	8
EP2C8F256C6	8256	203	165888	36	2	8

Package: FBGA
 Pin count: 256
 Speed grade: Fastest
 Core voltage: n/a
 Show advanced devices
 HardCopy compatible only

Companion device:
 HardCopy II:
 Limit DSP & RAM to HardCopy II device resources

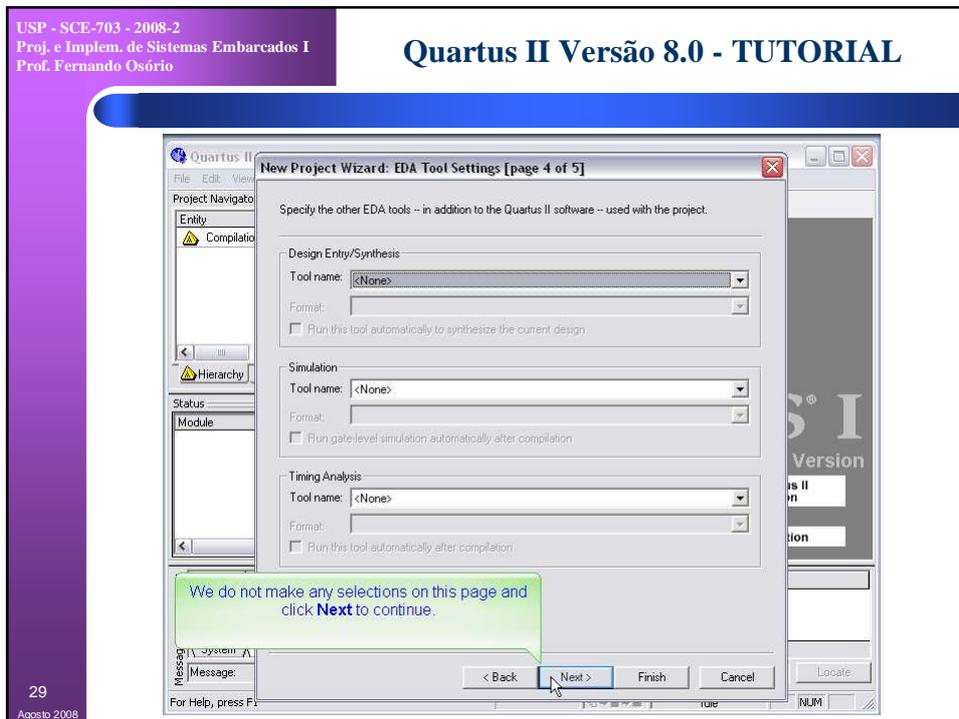
< Back Next > Finish Cancel

Finally, we select EP2C5F256C6 in the Available devices list.

28

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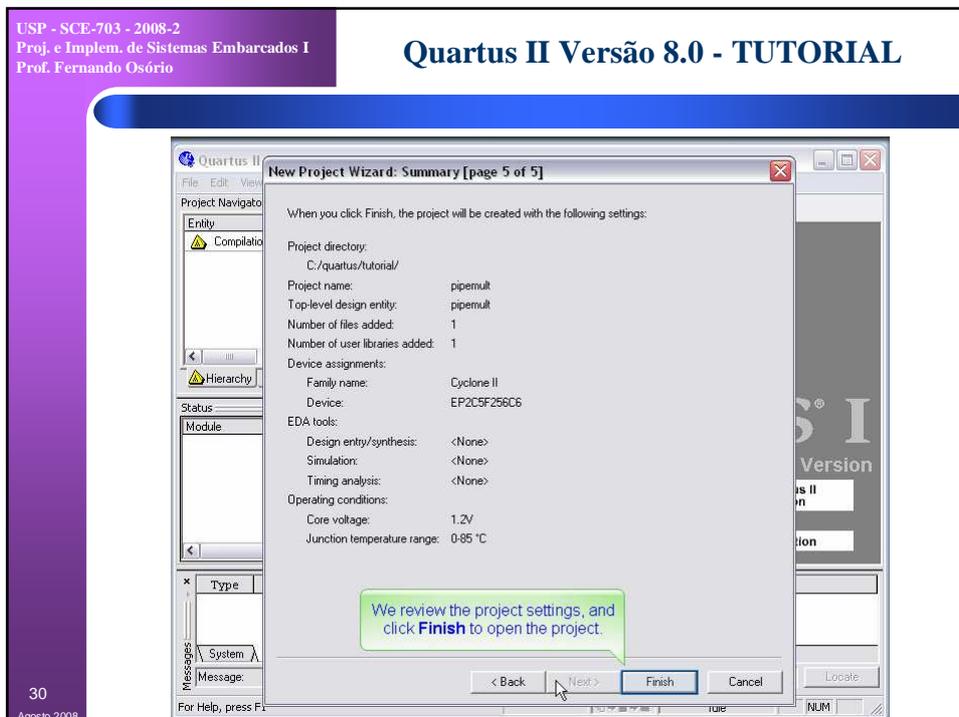
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29

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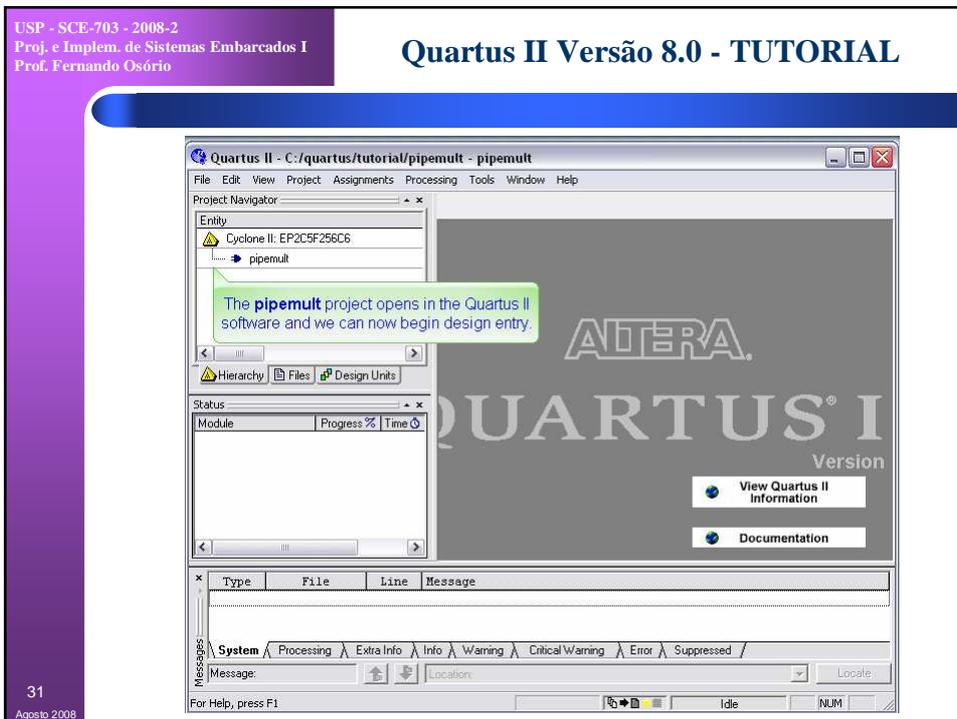
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30

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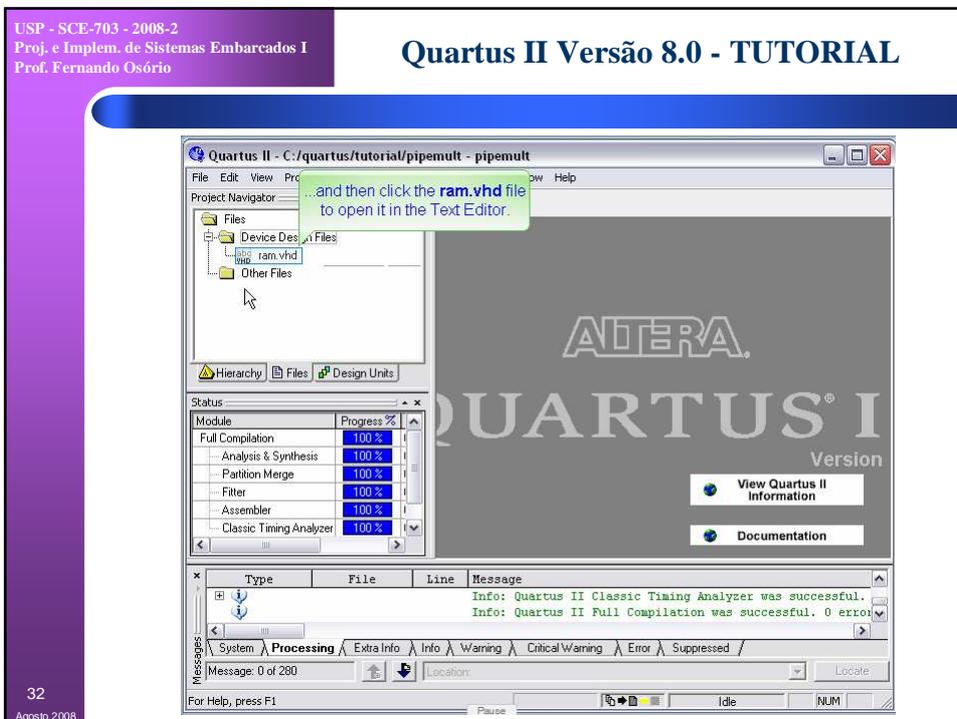
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31

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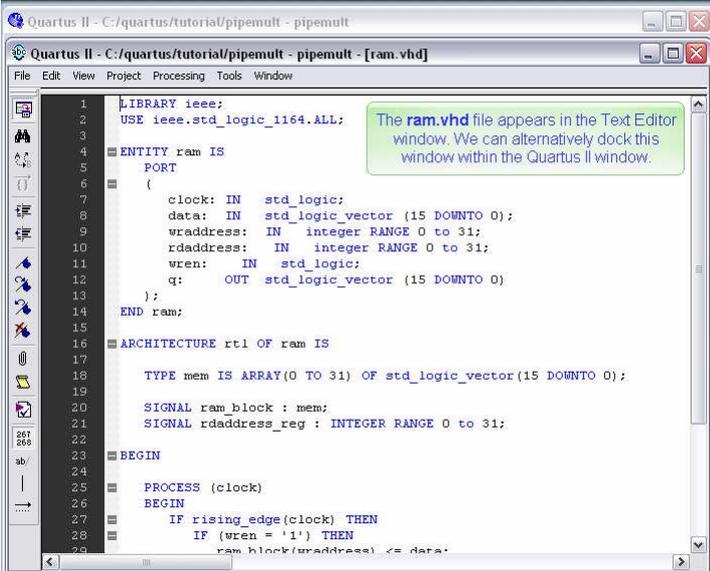
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32

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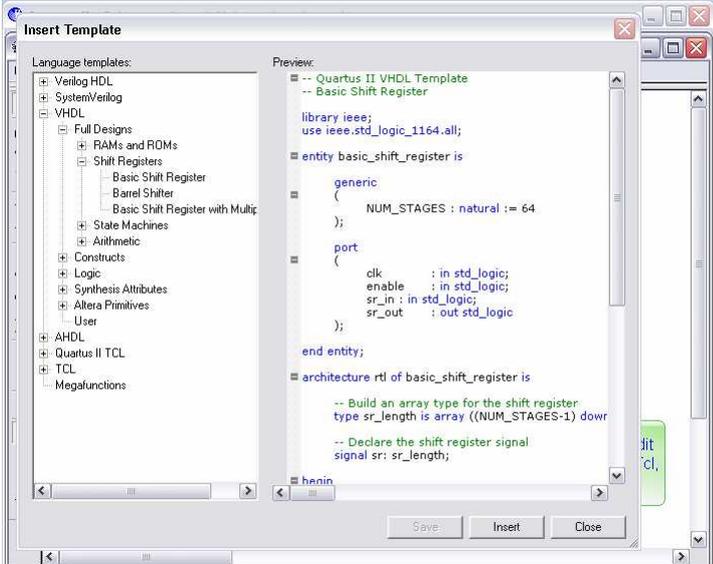
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The screenshot shows the Quartus II IDE with a VHDL code editor open. The code defines a RAM component named 'ram'. A green callout box points to the code with the text: "The ram.vhd file appears in the Text Editor window. We can alternatively dock this window within the Quartus II window." The code includes a library declaration, port definitions, and a behavioral process.

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3
4 ENTITY ram IS
5     PORT
6     (
7         clock: IN    std_logic;
8         data:  IN    std_logic_vector (15 DOWNTO 0);
9         wraddress: IN integer RANGE 0 to 31;
10        rdaddress: IN integer RANGE 0 to 31;
11        wren:   IN    std_logic;
12        q:     OUT   std_logic_vector (15 DOWNTO 0)
13    );
14 END ram;
15
16 ARCHITECTURE rtl OF ram IS
17
18     TYPE mem IS ARRAY(0 TO 31) OF std_logic_vector(15 DOWNTO 0);
19
20     SIGNAL ram_block : mem;
21     SIGNAL rdaddress_reg : INTEGER RANGE 0 to 31;
22
23 BEGIN
24
25     PROCESS (clock)
26     BEGIN
27         IF rising_edge(clock) THEN
28             IF (wren = '1') THEN
29                 ram_block(wraddress) <= data;
```

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The screenshot shows the 'Insert Template' dialog box in Quartus II. The left pane shows a tree view of language templates, with 'VHDL' expanded to 'Shift Registers' and 'Basic Shift Register' selected. The right pane shows a preview of the selected template's VHDL code. A green callout box points to the 'clock' signal in the code with the text: "clock".

```
-- Quartus II VHDL Template
-- Basic Shift Register

library ieee;
use ieee.std_logic_1164.all;

entity basic_shift_register is
    generic
    (
        NUM_STAGES : natural := 64
    );
    port
    (
        clk      : in std_logic;
        enable   : in std_logic;
        sr_in    : in std_logic;
        sr_out   : out std_logic;
    );
end entity;

architecture rtl of basic_shift_register is
    -- Build an array type for the shift register
    type sr_length is array ((NUM_STAGES-1) down
    to 0) of std_logic;
    -- Declare the shift register signal
    signal sr : sr_length;
```

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Step 2 - Create a Block Design File

This step shows you how to create a Block Design File with the Quartus II Block Editor.

Next

35

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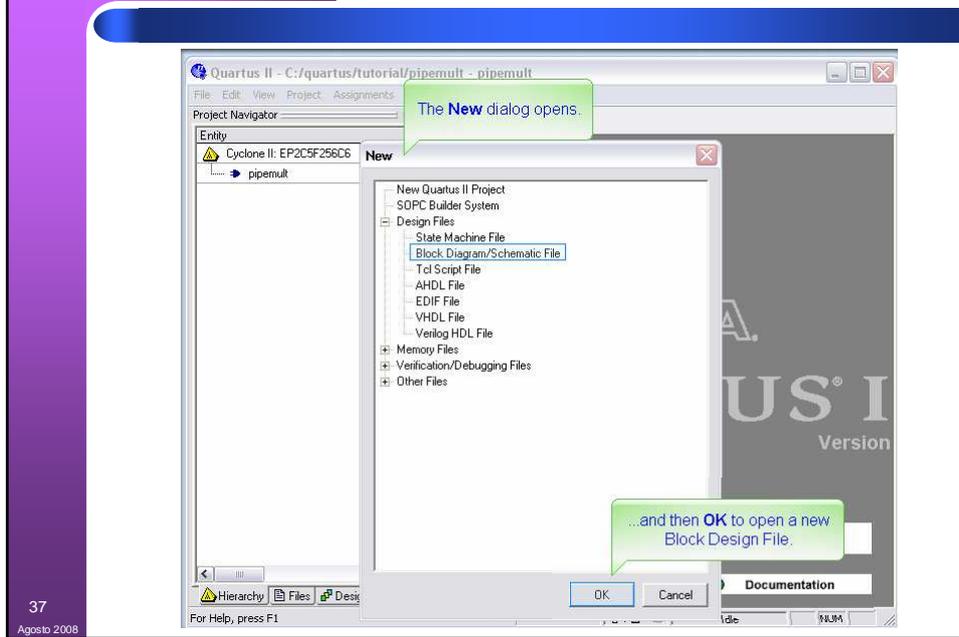
With the **pipemult** project open in Quartus II, we click the File menu.

...and then **New** to create a new Block Design File.

36

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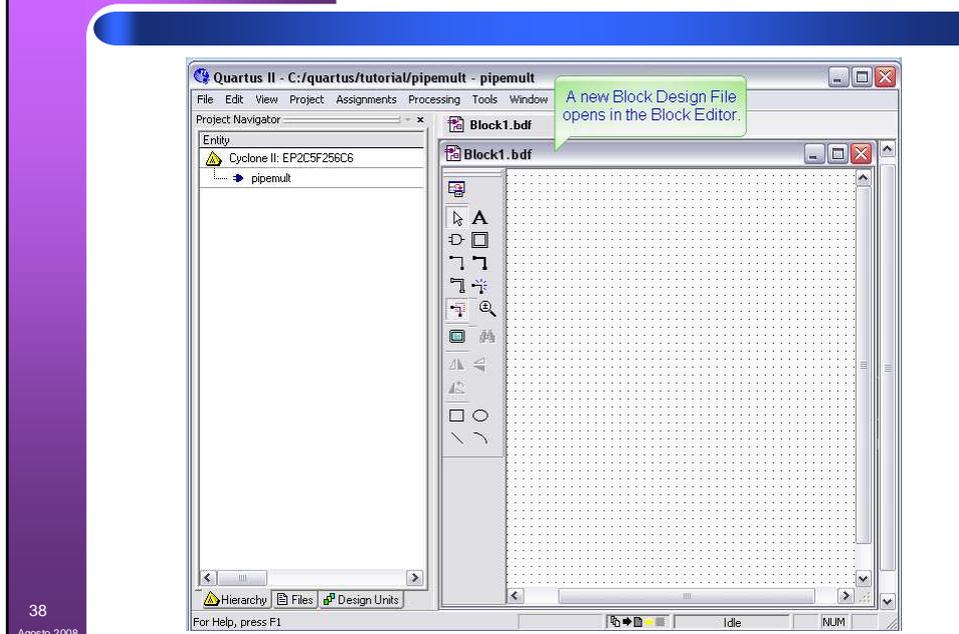
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37

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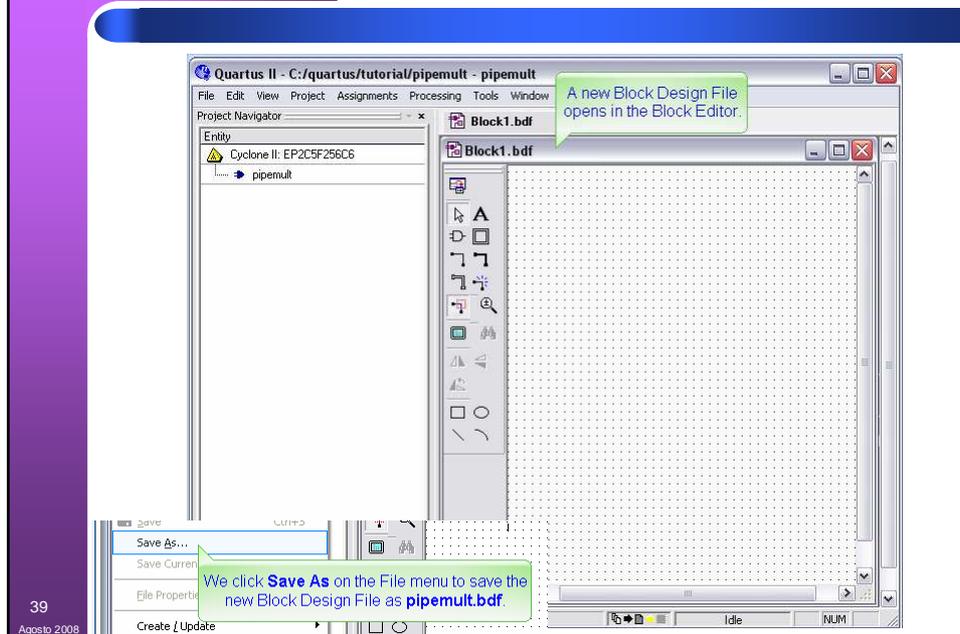
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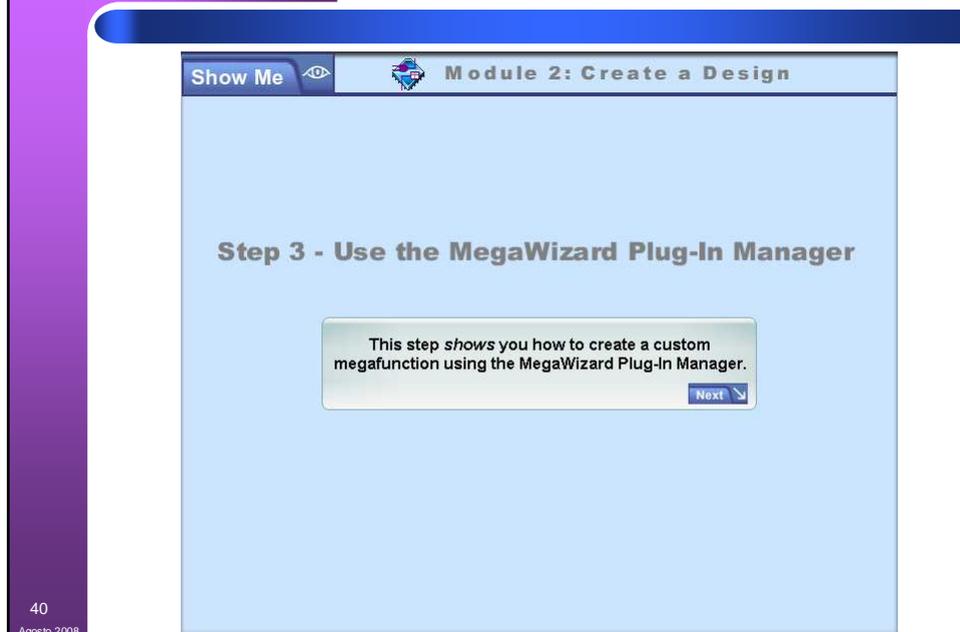
38

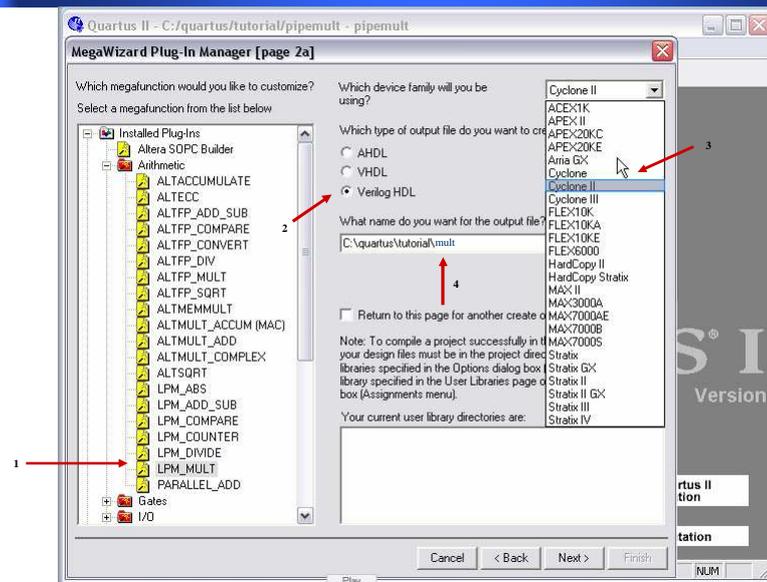
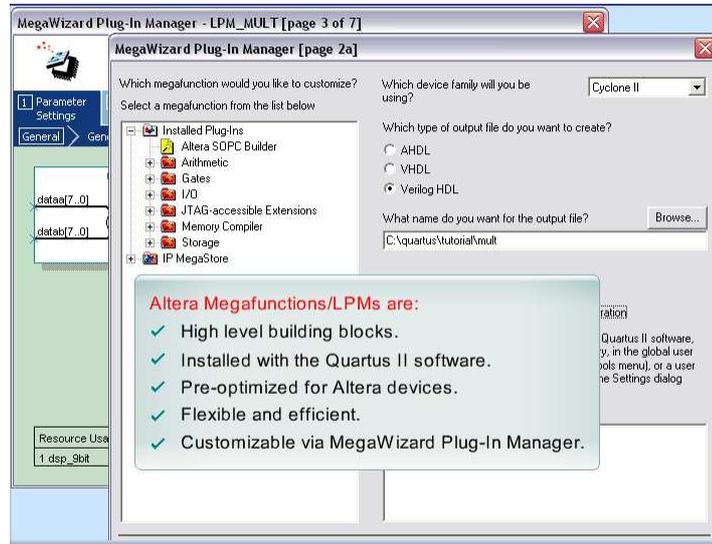
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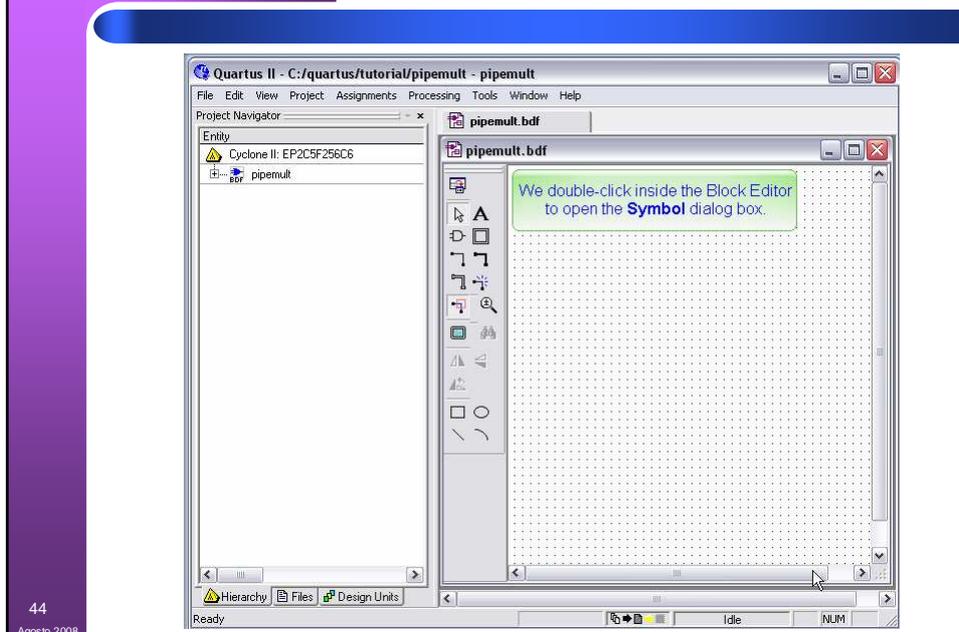
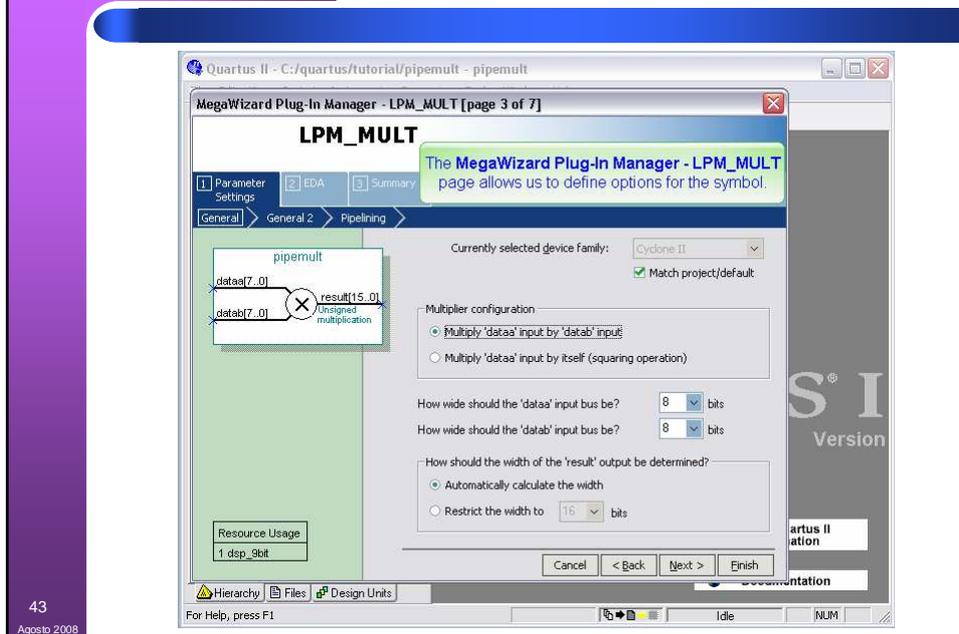
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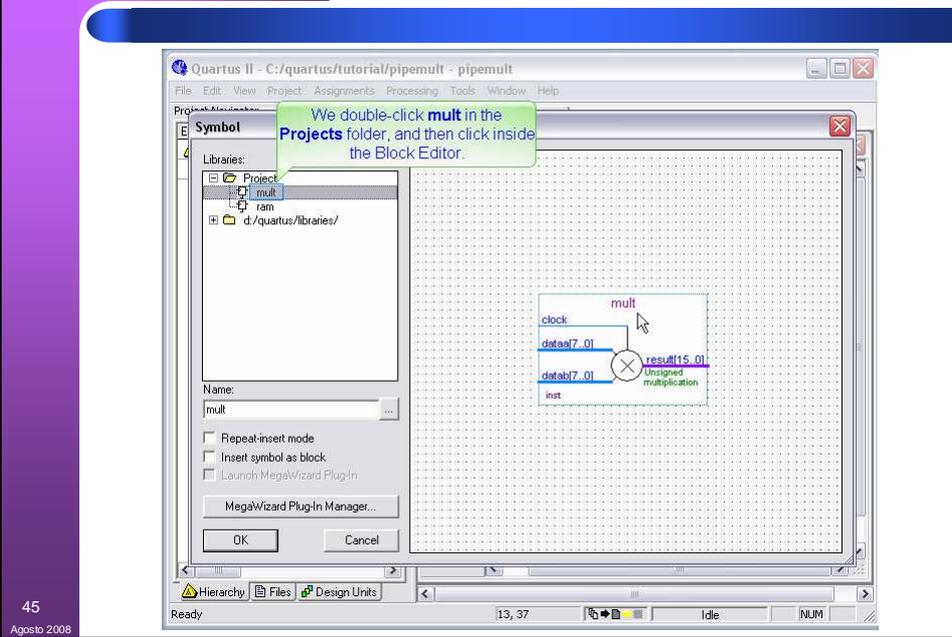


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Show Me 



Module 2: Create a Design

Step 5 - Add Pins

This step shows you how to create and connect pins in a schematic design.

[Next](#) 



QUARTUS® II
Interactive Tutorial



Module 3: Compile a Design

- Learning Objective -

Learn how to specify Compiler settings, run a full compilation, create a pin assignment, and analyze compilation results.

(Completion time = 40 minutes)

[Next](#) 



INFORMAÇÕES SOBRE A DISCIPLINA

USP - Universidade de São Paulo - São Carlos, SP
ICMC - Instituto de Ciências Matemáticas e de Computação
SSC - Departamento de Sistemas de Computação

Prof. Fernando Santos OSÓRIO

Web institucional: <http://www.icmc.usp.br/ssc/>

Página pessoal: <http://www.icmc.usp.br/~fosorio/>

E-mail: [fosorio \[at\] icmc. usp. br](mailto:fosorio@icmc.usp.br) ou [fosorio \[at\] gmail. com](mailto:fosorio@gmail.com)

Disciplina de Proj. e Implementação de Sistemas Embarcados I

Ferramentas: Altera - Quartus, NIOS II, Cyclone Dev-Kit

Web disciplina: <Http://www.icmc.usp.br/~fosorio/>

> Programa, Material de Aulas, Critérios de Avaliação,

> Material de Apoio, Trabalhos Práticos